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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,715	01/17/2002	Richard A. Olzak	H0001886	1380

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,715	OLZAK ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-31* is/are rejected.

7)☒ Claim(s) *3 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 0303
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Rejections Based On Prior Art

1. The following reference was relied upon for the rejections hereinbelow:

Okada et al. (US 6,5343,726 B1)

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 6, 10, 11, 16-18, 20, 21, 24, 25 and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada et al.

As to Claim 6, Okada et al. discloses, in Figs. 1-4: a PCB 11 having top and bottom layers 11A and 11B, respectively; a first footprint corresponding to component 12 on top layer 11A of PCB 11 for receiving component 12 (col.7: 8-11); a second footprint (pad portions of metallization 15) formed on the bottom layer 11B of PCB 11 for simulating a second surface mount device (for mounting to motherboard 5; Figs. 4 and 7); a plurality of I/O lines 16 connected between the first footprint and one or more of a plurality of electrical contacts (pad portions of metallization 15 formed on the bottom layer 11B of PCB 11) of the second footprint, at least a portion of each of the I/O lines

16 adjacent to the bottom layer and being exposed at through hole 15 between the top and bottom layers 11A and 11B. (col.7: 50-33).

As to Claim 10, Okada et al. discloses each of I/O lines 16 comprises a quantity of electrically conductive metal 15 deposited in a groove 14 communicating between layers 11A and 11B (Fig. 4).

As to Claim 11, Okada et al. discloses, in Fig. 1, that the first footprint (corresponding to component 12) is different than the second footprint (pad portions of metallization 15 formed on the bottom layer 11B of PCB 11 and shown in Fig. 4).

As to Claims 16 and 20, Okada et al. discloses, in Figs. 1-4: a body means 11 supporting device 12 relative to PCB 5 (col.7: 8-12); a first interconnecting means corresponding to surface mount device 12 on first surface 11A for interconnecting device 12 (col.7: 8-11); a second interconnecting means (pad portions of metallization 15 formed on a second surface 11B of body means 11) for electrically interconnecting to a PCB 5 structured to receive a second surface mounted device (i.e., body means 11; Fig. 7); means 13 for electrically coupling the first and second interconnecting means, at least a portion 15 of the coupling means 13 being exposed between the first and second surfaces 11A and 11B of body means 11 (Figs. 1 and 4).

As to Claim 17, Okada et al. discloses signal communication means 17 spanning between the first and second surfaces 11A and 11B.

As to Claim 18, Okada et al. discloses the exposed portion 15 of the electrical coupling is positioned adjacent to the second surface 11B of body means 11 (Fig. 4).

As to Claim 21, Okada et al. discloses providing at least a portion of the second electrical connecting means 13; i.e., the bottom layer pads of metallization 15, along an exterior surface (layer 11B) of body 11.

As to Claim 24, Okada et al. discloses forming a quantity of contacts (pad portions of metallization 15) on the bottom layer 11B (Fig. 4) in a structured pattern simulating I/O leads of the second surface mounted device mounted to PCB 5 (Fig. 7; col.7: 11-12; col.8: 25-30).

As to Claim 25, Okada et al. discloses soldering the contacts on the bottom layer 11B of body 11 to solder pads on PCB 5 corresponding to I/O leads of the second surface mounted device (Figs. 7 and 8; col.7: 11-12; col.8: 25-30).

As to Claim 27, Okada et al. discloses, in Figs. 1-4: a PCB 11 having top and bottom layers 11A and 11B, respectively; a first footprint corresponding to component 12 and formed on top layer 11A of PCB 11 (Fig. 1; col.7: 8-11); a first surface mount device 12 mounted to the footprint on top layer 11A (col.7: 8-11); a plurality of signal carriers 13 positioned along different peripheral edges of PCB 11 (Fig. 1) and extended between top and bottom layers 11A and 11B; signal carriers 13 being at least partially exposed in an area adjacent to bottom layer 11B, each of signal carriers 13 being electrically and mechanically joined to a corresponding contact area (corresponding to component 12) of PCB 11 (Fig. 1); a plurality of signal lines 16 communicating between the corresponding contact areas of the footprint and at least a portion of the signal carriers 13 (Figs. 1 and 4).

As to Claim 28, Okada et al. discloses a contact pad (corresponding to the pad portion of signal line metallization 15; Fig. 4) formed on the bottom layers 11B at each of the signal carriers 13.

As to Claim 29, Okada et al. discloses solder joint 17 joined to corresponding contact areas of PCB 5, each joint left partially formed on the partially exposed portion of each of the signal carriers (Figs. 1 and 4-7).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4, 5, 7-9, 12-15, 19, 22, 23, 26, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al.

As to Claim 1:

I. Okada et al. discloses, in Figs. 1-4: insulating body 11; offset first and second surface 11A and 11B, respectively; a pattern of surface mount pads formed on first surface 11A corresponding to component 12 (col.7: 8-11); a pattern of signal carriers 13 at least partially exposed in an area between surfaces 11A and 11B and adjacent to the second surface 11B; signal lines 16 electrically coupling one or more of the surface mount pads with predetermined ones of signal carriers 13 (col.7: 30-33).

II. Okada et al. does not teach that the surface mount pads corresponding to component 12 are solder pads.

III. However, solder mounting a leaded or bumped electronic component to solder pads is an old and well-known surface mounting technique in the electronics art and it would have been obvious to one of ordinary skill in the art at the time of the invention to use the surface mount pads as solder pads in order to form a reliable electromechanical connection of the electronic component 12 to insulating body 11.

As to Claim 2, Okada et al. discloses a pattern of electrical contacts continuous with end-face electrode 15 on second surface 11B and being electrically coupled different ones of signal carriers 13 (Figs. 4 and 7).

As to Claim 4,Okada et al. discloses electrically conductive material 15 formed on an interior surface of a passage 14 that communicates between surfaces 11A and 11B (Fig. 4; col.7: 15-18 and 27-28).

As to Claims 5, 26, 30 and 31:

I. Okada et al. discloses that signal lines 16 couple a function of a surface mount device (which could function as a replacement for another) to a signal carrier 13 that corresponds to a position in the pattern of signal carriers 13.

II. Okada et al. does not teach specific functions of the signal carriers 13 or the electronic component 12.

III. However, it would have been obvious to one of ordinary skill in the art to assign the various signal, ground, power, or other functional pins of the surface mount component 12 to the appropriate signal carriers 13, in particular to a signal carrier 13

assigned with a similar function as the particular corresponding pin of component 12 in order to transmit that functional information to the motherboard 5 (Fig. 7) to meet the requirements of the particular electronic system application.

As to Claim 7:

I. Okada et al. discloses a pattern of surface mount pads formed on first surface 11A corresponding to the first footprint receiving component 12 (col.7: 8-11) but does not teach that the surface mount pads corresponding to the footprint are solder pads.

II. However, solder mounting a leaded or bumped electronic component to solder pads is an old and well-known surface mounting technique in the electronics art and it would have been obvious to one of ordinary skill in the art at the time of the invention to use the surface mount pads, corresponding to the footprint, as solder pads in order to form a reliable electromechanical connection of the electronic component 12 to PCB 11.

As to Claim 8, Okada et al. discloses the I/O lines 16 couple one or more of the solder pads on the top layer to one or more of the plurality of electrical contacts (pad portions of metallization 15) on the bottom layer 11B (Fig. 4).

As to Claim 9, Okada et al. discloses a plurality of solder pads (pad portions of metallization 15) on bottom layer 11B and corresponding to the second footprint (Figs. 4, 7 and 8).

As to Claim 12:

I. Okada et al. discloses, in Figs. 1-4: a PCB 11 having a top and bottom layer 11A and 11B, respectively; a pattern of surface mount pads formed on top layer 11A

structured for receiving a first surface mount device 12 (col.7: 8-11); a plurality of vias 13 formed along the periphery of PCB 11 and communicating between top and bottom layers 11A and 11B, each of vias 13 having a quantity of electrically conductive material 17 deposited therein (Figs. 1 and 4; col.7: 35-37); an electrical signal line 16 coupled between one of the surface mount pads and one of vias 13 (Figs. 1 and 2); a pattern of electrical contacts (pad portions of metallization 15) on the bottom layer 11B of PCB 11 (Fig. 4), the pattern structured to simulate a second surface mount device (Fig. 7; col. 7: 11-12).

II. Okada et al. does not teach that the surface mount pads corresponding to component 12 are solder pads.

III. However, solder mounting a leaded or bumped electronic component to solder pads is an old and well-known surface mounting technique in the electronics art and it would have been obvious to one of ordinary skill in the art at the time of the invention to use the surface mount pads as solder pads in order to form a reliable electromechanical connection of the electronic component 12 to insulating body 11.

As to Claim 13, Okada et al. discloses at least a portion of the conductive material 17 in each of vias 13 adjacent to the contacts formed on bottom layer 11B is exposed between the top and bottom layers 11A and 11B (Fig. 2).

As to Claim 14, Okada et al. further discloses an electrically conductive material 15 plated on an interior surface of a partial cylindrical passage 14 (Fig. 4; col.12: 10-13).

As to Claim 15, Okada et al. discloses a plurality of interconnected layers (col.6 : 66-col.7 : 3) including a ground layer for grounding certain pins of the component 12

(col.1: 51-54) and, inherently, a signal layer for carrying the signals to and from the component 12.

As to Claims 19, 22 and 23:

II. Okada et al. does not teach that the first interconnecting means further comprises means for forming an electrically conductive solder joint.

III. However, solder mounting a leaded or bumped electronic component to solder pads using solder joints is an old and well-known surface mounting technique in the electronics art and it would have been obvious to one of ordinary skill in the art at the time of the invention to use the surface mount pads as solder pads in order to form a reliable electromechanical (solder joint) connection of the electronic component 12 to body means 11.

Allowable Subject Matter

6. Claims 3 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 3, patentability resides in *a signal layer laminated between the first and second surfaces with one or more of the plurality of signal lines being formed on the signal layer*, in combination with the other limitations of the claim.

As to Claim 32, patentability resides in *fewer of the corresponding contact areas of the footprint are provided for the replacement device than the contact areas provided on the printed circuit board for the replaced device*, in combination with the other limitations of the claim.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bedos et al. (US 6,031,728) discloses an adapter body 1 with signal carriers 17 (Fig. 1).

Terashima et al. (US 6,452,112 B1) discloses an interconnection board 7 with signal carriers 3, said board 7 being mounted on a motherboard 8 (Figs. 3-5).

Wakely (US 3,483,308) discloses a ceramic chip carrier 12 with signal carriers 26, said carrier 12 mounted on a motherboard 32 (Figs. 1, 2 and 4).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
June 30, 2003